

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Methods For Forming Wordlines, Transistor Gates,  
And Conductive Interconnects, And Wordline,  
Transistor Gate, And Conductive Interconnect  
Structures

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ATTORNEY'S DOCKET NO. MI22-532

## TECHNICAL FIELD

The invention pertains to a number of semiconductor structures and methods for forming such structures, including gate stack structures, conductive line structures, conductive interconnect structures, and programmable-read-only-memory devices.

## BACKGROUND OF THE INVENTION

A continuous challenge in semiconductor processing is to improve conductivity and performance of stacked semiconductor structures. Among the stacked semiconductor structures commonly utilized are gate stacks, wordlines, programmable-read-only-memory devices such as EPROMs and EEPROMs, and conductive interconnects. Formation of some of these prior art stacked structures is described with reference to Figs. 1-4. Figs. 1-2 pertain to the formation of a wordline or gate stack structure, and Figs. 3-4 pertain to the formation of a programmable-read-only memory device.

Referring to Fig. 1, a semiconductor wafer fragment 10 is illustrated at a preliminary processing step of a prior art process for forming a wordline or gate stack. Wafer fragment 10 comprises a semiconductive material substrate 12, and field oxide regions 14 over substrate 12. A gate dielectric layer 16, generally comprising silicon dioxide, extends between field oxide regions 14. A polysilicon layer 18

1 and a polycide (silicide) layer 20 are formed over field oxide regions 14  
2 and gate dielectric layer 16.

3 Polysilicon layer 18 typically comprises polysilicon uniformly doped  
4 with a conductivity enhancing dopant (illustrated by stippling within  
5 layer 18). Polycide layer 20 comprises a metal silicide, such as tungsten  
6 silicide, molybdenum silicide, titanium silicide or cobalt silicide. The  
7 formation of polycide layer 20 typically comprises depositing a metal over  
8 polysilicon layer 18 and reacting the metal with polysilicon layer 18 to  
9 form a metal-silicide. The reacting can comprise thermal processing of  
10 the metal layer and polysilicon layer at, for example, temperatures of  
11 from about 600°C to about 800°C.

12 Referring to Fig. 2, layers 16, 18 and 20 are patterned to form a  
13 conductive stack, and specifically to form a wordline 24. Source/drain  
14 regions 25 are provided proximate wordline 24. Conductive wordline 24  
15 comprises a transistor gate electrically connecting source/drain regions 25.  
16 The final transistor structure can be either a p-channel transistor  
17 (PMOS), or an n-channel transistor (NMOS), and can be incorporated  
18 within a CMOS construction.

19 The speed of devices comprising wordlines and conductive gates  
20 generally increases with increasing conductivities of the wordlines and  
21 conductive gates. Accordingly, it would be desirable to improve the  
22 conductivity of wordlines and transistor gates. A method for improving  
23 the conductivity of a doped layer is to "activate" the dopant within the

1 layer. Although the chemistry of dopant activation is not well  
2 understood, activation is thought to occur as dopant is dispersed from  
3 grain boundaries in a polysilicon layer to bulk polysilicon away from the  
4 grain boundaries. Dopants are typically activated by thermal processing.

5 Alternative procedures similar to those of Figs. 1 and 2 can be  
6 used to form a conductive polysilicon interconnect. Such interconnects  
7 can comprise a line of polycide over a polysilicon. Accordingly, such  
8 interconnects are similar to wordline 24, but lack dielectric layer 16.

9 The speed of devices comprising conductive interconnects can  
10 increase with increasing conductivities of the conductive interconnects.  
11 Accordingly, it would be desirable to improve the conductivity of  
12 conductive interconnects.

13 Referring to Figs. 3-4, a prior art process for forming a  
14 programmable-read-only memory (PROM) device is illustrated. In the  
15 embodiment of Figs. 3-4, similar numbering to that of the embodiment  
16 of Figs. 1-2 is utilized, with differences indicated by the suffix "a", or by  
17 different numbers.

18 Referring to Fig. 3, a wafer fragment 10a is illustrated at a  
19 preliminary step during formation of a programmable-read-only memory  
20 device. Wafer fragment 10a comprises a semiconductive material 12a  
21 over which is formed field oxide regions 14a and gate dielectric  
22 layer 16a. A first polysilicon layer 18a is formed over regions 14a and  
23 dielectric layer 16a. A second dielectric layer 26 and a second

1 polysilicon layer 28 are formed over first polysilicon layer 18a, and a  
2 polycide layer 30 is formed over second dielectric layer 26.

3 Polysilicon layers 18a and 28 comprise uniformly doped polysilicon,  
4 typically comprising a dopant concentration of greater than  
5  $1 \times 10^{19}$  ions/cm<sup>3</sup>.

6 Referring to Fig. 4, layers 16a, 18a, 20a, 26, 28 and 30 are  
7 patterned to form the resulting PROM device 32. Within device 32, the  
8 patterned first polysilicon layer 18a is typically referred to as a floating  
9 gate. The patterned second polysilicon layer 28 and polycide layer 30  
10 together comprise a conductive line 33.

11 The speed of circuits comprising PROM devices can increase with  
12 increasing conductivities of the conductive line and floating gate.  
13 Accordingly, it would be desirable to improve the conductivities of  
14 conductive lines and floating gates.

## SUMMARY OF THE INVENTION

The invention encompasses stacked semiconductor devices including gate stacks, wordlines, PROMs, conductive interconnecting lines, and methods for forming such structures.

In one aspect, the invention includes a method of forming a conductive line. A silicide layer is formed against a polysilicon layer. A conductivity-enhancing impurity is provided within the silicide layer. The polysilicon layer and the silicide layer are formed into a conductive line shape.

In another aspect, the invention includes a programmable-read-only-memory device comprising a first dielectric layer over a substrate, a floating gate over the first dielectric layer, a second dielectric layer over the floating gate, a conductive line over the second dielectric layer, and a metal-silicide layer over the conductive line. The metal-silicide layer comprises a Group III dopant or a Group V dopant.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 illustrates a semiconductor wafer fragment at preliminary step of a prior art method for forming a wordline.

Fig. 2 illustrates the Fig. 1 wafer fragment at a prior art step subsequent to that of Fig. 1.

1           Fig. 3 illustrates a semiconductor wafer fragment at preliminary  
2 step of a prior art method for forming PROM device.

3           Fig. 4 illustrates the Fig. 3 wafer fragment at a prior art step  
4 subsequent to that of Fig. 3.

5           Fig. 5 illustrates a semiconductor wafer fragment at preliminary  
6 step of a first embodiment method of the present invention for forming  
7 a wordline.

8           Fig. 6 illustrates the Fig. 5 wafer fragment at a step subsequent  
9 to that of Fig. 5.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A first embodiment of the present invention is described with reference to Figs. 5 and 6. In describing the first embodiment, like numerals from the preceding discussion of the prior art are utilized where appropriate, with differences being indicated by the suffix "b" or with different numerals.

Referring to Fig. 5, a semiconductor wafer fragment 10b is illustrated at a preliminary processing step. Wafer fragment 10b comprises a semiconductive material substrate 12b, such as, for example, monocrystalline silicon. Field isolation regions 14b and a gate dielectric layer 16b are formed over semiconductive material 12b. Field isolation regions 14b and gate dielectric layer 16b comprise an insulative material, such as, for example, silicon dioxide.

A conductive layer 18b and a polycide layer 20b are formed over field isolation regions 14b and gate dielectric layer 16b. Conductive layer 18b preferably comprises polysilicon doped to a concentration of greater than  $1 \times 10^{19}$  atoms/cm<sup>3</sup> with a conductivity enhancing dopant. Polycide layer 20b is against conductive layer 18b and comprises a metal silicide doped with conductivity enhancing dopant (the dopant being indicated by stippling). Preferably, polycide layer 20b is doped to a



1 concentration of greater than  $1 \times 10^{18}$  atom/cm<sup>3</sup> with the conductivity  
2 enhancing dopant.

3 Polycide layer 20b can comprise, for example, a metal selected  
4 from the group consisting of tungsten, tantalum, titanium, molybdenum  
5 and cobalt. Polycide layer 20b can be formed by the prior art method  
6 of depositing a metal over polysilicon layer 18b and reacting the metal  
7 with polysilicon layer 18b at temperatures of from about 600°C to about  
8 800°C to form silicide layer 20b. Alternatively, and preferably, the  
9 thermal processing to form polycide layer 20b encompasses rapid thermal  
10 processing (RTP). In the context of this document, RTP refers to a  
11 process wherein a temperature is ramped at greater than about  
12 7°C/second. Preferably, the RTP temperature is ramped to exceed 850°C  
13 and is maintained above 850°C for at least 10 seconds. Such RTP can  
14 activate dopant within polycide layer 20b to increase the conductivity of  
15 doped polycide layer 20b.

16 The RTP preferably occurs while exposing silicide layer 20b to an  
17 oxygen-comprising atmosphere, such as, for example, an atmosphere  
18 comprising at least one compound selected from the group consisting of  
19 O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub>O and NO. Under such preferred conditions, a silicon dioxide  
20 layer 35 can be formed over polycide layer 20b. Silicon dioxide layer 35  
21 can impede or prevent dopant diffusion outwardly from layer 20b and  
22 thereby advantageously retain dopant within layer 20b. It is noted that  
23 while the RTP preferably occurs while exposing layer 20b to an oxidizing

1 atmosphere, the RTP will generally also activate dopant within layer 20b  
2 if conducted while exposing layer 20b to a non-oxidizing atmosphere.

3 Wafer 10b differs from wafer 10 of the prior art (shown in Figs. 1  
4 and 2) in that polycide layer 20b is doped with a conductivity-enhancing  
5 impurity, whereas the prior art polycide 20 (shown in Figs. 1 and 2) is  
6 not doped. As indicated above, the conductivity-enhancing dopant is  
7 preferably provided to a concentration of greater than  $1 \times 10^{18}$  atom/cm<sup>3</sup>.  
8 Suitable conductivity enhancing dopants can comprise, for example, Group  
9 III or Group V dopants, such as dopants comprising boron, phosphorous  
10 or arsenic. Methods for doping silicide layer 20b include, for example,  
11 implanting dopant into the layer after formation/deposition of the layer,  
12 *in situ* doping of the layer during either chemical vapor deposition  
13 (CVD) or sputter deposition, and out-diffusion from a doped polysilicon  
14 layer 18b beneath silicide layer 20b.

15 An example CVD process for forming a polycide layer 20b  
16 comprising tungsten silicide doped with phosphorus ( $\text{WSi}_x\text{P}_y$ ) comprises  
17 utilization of  $\text{WF}_6$ ,  $\text{SiH}_4$  and  $\text{PH}_3$  as precursor materials in a CVD  
18 reactor. Alternatively, dichlorosilane can be substituted for  $\text{SiH}_4$ . Also,  
19 alternative dopant hydrides can be substituted for  $\text{PH}_3$  to form a polycide  
20 doped with an alternative dopant. Such alternative metal hydrides can  
21 include, for example,  $\text{AsH}_3$  or diborane. Also, other organic precursors  
22 comprising Group III or Group V dopants can be utilized as alternative  
23 sources of dopant.

1       An example sputter deposition process comprises utilization of a  
2       target comprising a mixture of a source of metal, a source of silicon and  
3       a source of conductivity-enhancing impurity. The target is sputtered to  
4       form a silicide layer 20b comprising the conductivity-enhancing impurity  
5       and the metal.

6       Referring to Fig. 6, layers 16b, 18b, 20b, and 35 are patterned to  
7       form a conductive line 24b. Source/drain regions 25b are formed within  
8       substrate 12b such that conductive line 24b comprises a stacked transistor  
9       gate structure which electrically connects source/drain regions 25b. The  
10      resulting transistor structure can be a PMOS transistor or NMOS  
11      transistor, and can be incorporated into a CMOS structure.

12      Conductive line 24b differs from conductive line 24 (shown in  
13      Fig. 2) in that line 24b comprises a silicide layer 20b doped with  
14      conductivity-enhancing impurity. Such doping of layer 20b can lower the  
15      resistance of layer 20b relative to that of layer 20 (shown in Fig. 1) and  
16      thereby improve the performance of conductive line 24b relative to that  
17      of conductive line 24 (shown in Fig. 2). The above-discussed RTP can  
18      further improve the conductivity of layer 20b by activating dopant within  
19      layer 20b.

20      Although layer 20b is doped prior to patterning of layer 20b to  
21      form wordline 24b in the shown method, in alternative embodiments layer  
22      20b can be doped after such patterning. As an example method of  
23      accomplishing such alternative embodiments, layer 20b could be doped by

1 ion implanting a conductivity enhancing dopant into layer 20b after  
2 patterning of layer 20b to form wordline 24b. As another example  
3 method, layer 20b can be doped by out-diffusion from conductively doped  
4 layer 18b by thermal treatment of wordline 24b.

5 The doped silicide of the present invention can be incorporated  
6 into numerous circuit device structures, including, for example,  
7 programmable-read-only-devices such as EPROMS and EEPROMS.

8 To aid in interpretation of the claims that follow, the term  
9 "semiconductive substrate" is defined to mean any construction comprising  
10 semiconductive material, including, but not limited to, bulk  
11 semiconductive materials such as a semiconductive wafer (either alone or  
12 in assemblies comprising other materials thereon), and semiconductive  
13 material layers (either alone or in assemblies comprising other materials).  
14 The term "substrate" refers to any supporting structure, including, but not  
15 limited to, the semiconductive substrates described above.

16 In compliance with the statute, the invention has been described  
17 in language more or less specific as to structural and methodical  
18 features. It is to be understood, however, that the invention is not  
19 limited to the specific features shown and described, since the means  
20 herein disclosed comprise preferred forms of putting the invention into  
21 effect. The invention is, therefore, claimed in any of its forms or  
22 modifications within the proper scope of the appended claims  
23 appropriately interpreted in accordance with the doctrine of equivalents.